19-0605; Rev 0; 8/06

MAXIM

# Single-/Dual-/Triple-Voltage µP Supervisory Circuits with Independent Watchdog Output



## General Description

The MAX6730A–MAX6735A single-/dual-/triple-voltage microprocessor (µP) supervisors feature a watchdog timer and manual reset capability. The MAX6730A–MAX6735A offer factory-set reset thresholds for monitoring voltages from +0.9V to +5V and an adjustable reset input for monitoring voltages down to +0.63V. The combination of these features significantly improves system reliability and accuracy when compared to separate ICs or discrete components.

The active-low reset output asserts and remains asserted for the reset timeout period after all the monitored voltages exceed their respective thresholds. Multiple factory-set reset threshold combinations reduce the number of external components required. The MAX6730A/MAX6731A monitor a single fixed voltage, the MAX6732A/MAX6733A monitor two fixed voltages, and the MAX6734A/MAX6735A monitor two fixed voltages and one adjustable voltage. All devices are offered with six minimum reset timeout periods ranging from 1.1ms to 1120ms.

The MAX6730A–MAX6735A feature a watchdog timer with an independent watchdog output. The watchdog timer prevents system lockup during code execution errors. A watchdog startup delay of 54s after reset asserts allows system initialization during power-up. The watchdog operates in normal mode with a 1.68s delay after initialization. The MAX6730A/MAX6732A/MAX6734A provide an active-low, open-drain watchdog output. The MAX6731A/MAX6733A/MAX6735A provide an active-low, push-pull watchdog output.

Other features include a manual reset input (MAX6730A/MAX6731A/MAX6734A/MAX6735A) and push-pull reset output (MAX6731A/MAX6733A/MAX6735A) or open-drain reset output (MAX6730A/MAX6732A/MAX6734A). The MAX6730A–MAX6733A are offered in a tiny 6-pin SOT23 package. The MAX6734A/MAX6735A are offered in an 8-pin, space-saving SOT23 package. All devices are fully specified over the extended -40°C to +125°C temperature range.

## Applications

Multivoltage Systems
Telecom/Networking Equipment
Computers/Servers
Portable/Battery-Operated Equipment
Industrial Equipment
Printer/Fax
Set-Top Boxes

***Typical Operating Circuit and Pin Configurations appear at end of data sheet.***

## Features

- **$V_{CC}1$ (Primary Supply) Reset Threshold Voltages from +1.575V to +4.63V**
- **$V_{CC}2$ (Secondary Supply) Reset Threshold Voltages from +0.79V to +3.08V**
- **Adjustable RSTIN Threshold for Monitoring Voltages Down to +0.63V (MAX6734A/MAX6735A Only)**
- **Six Reset Timeout Options**
- **Watchdog Timer with Independent Watchdog Output**
  **35s (min) Initial Watchdog Startup Period**
  **1.12s (min) Normal Watchdog Timeout Period**
- **Manual Reset Input (MAX6730A/MAX6731A/MAX6734A/MAX6735A)**
- **Guaranteed Reset Valid down to $V_{CC}1$ or $V_{CC}2$ = +0.8V**
- **Push-Pull $\overline{RESET}$ or Open-Drain $\overline{RESET}$ Output**
- **Immune to Short $V_{CC}$ Transients**
- **Low Supply Current: 14µA (typ) at +3.6V**
- **Small 6-Pin and 8-Pin SOT23 Packages**

## Ordering Information

| PART* | PIN-PACKAGE | PKG CODE |
|---|---|---|
| **MAX6730A**UT_D_ -T | 6 SOT23-6 | U6-1 |
| **MAX6731A**UT_D_ -T | 6 SOT23-6 | U6-1 |
| **MAX6732A**UT_ _D_ -T | 6 SOT23-6 | U6-1 |
| **MAX6733A**UT_ _D_ -T | 6 SOT23-6 | U6-1 |
| **MAX6734A**KA_ _D_ -T | 8 SOT23-8 | K8S-3 |
| **MAX6735A**KA_ _D_ -T | 8 SOT23-8 | K8S-3 |

*All devices specified over the -40°C to +125°C operating temperature range.*

***Note:** *Insert the threshold level suffixes for $V_{CC}1$ and $V_{CC}2$ (Table 1) after "UT" or "KA." For the MAX6730A/MAX6731A, insert only the $V_{CC}1$ threshold suffix after the "UT." Insert the reset timeout delay (Table 2) after "D" to complete the part number. For example, the MAX6732AUTLTD3-T provides a $V_{CC}1$ threshold of +4.625V, a $V_{CC}2$ threshold of +3.075V, and a 210ms reset timeout period. Sample stock is generally held on standard versions only (see the Standard Versions table). Standard versions have an order increment requirement of 2500 pieces. Nonstandard versions have an order increment requirement of 10,000 pieces. Contact factory for availability. Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing "T" with "+T" when ordering.*



***For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.***

# Single-/Dual-/Triple-Voltage µP Supervisory Circuits with Independent Watchdog Output

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}1$, $V_{CC}2$, RSTIN, $\overline{MR}$, WDI to GND .....-0.3V to +6V
$\overline{RST}$, $\overline{WDO}$ to GND (open drain).....-0.3V to +6V
$\overline{RST}$, $\overline{WDO}$ to GND (push-pull).....-0.3V to ($V_{CC}1$ + 0.3V)
Input Current/Output Current (all pins) .....20mA
Continuous Power Dissipation ($T_A$ = +70°C)
6-Pin SOT23-6 (derate 8.7mW/°C above +70°C) .....696mW
8-Pin SOT23-8 (derate 8.9mW/°C above +70°C) .....714mW
Operating Temperature Range .....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}1$ = $V_{CC}2$ = +0.8V to +5.5V, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}1$, $V_{CC}2$ | | 0.8 | | 5.5 | V |
| Supply Current | $I_{CC}1$ | $V_{CC}1$ < +5.5V, all I/O connections open, outputs not asserted | | 15 | 39 | µA |
| | | $V_{CC}1$ < +3.6V, all I/O connections open, outputs not asserted | | 10 | 28 | |
| | $I_{CC}2$ | $V_{CC}2$ < +3.6V, all I/O connections open, outputs not asserted | | 4 | 11 | |
| | | $V_{CC}2$ < +2.75V, all I/O connections open, outputs not asserted | | 3 | 9 | |
| $V_{CC}1$ Reset Threshold | $V_{TH}1$ | L (falling) | 4.500 | 4.625 | 4.750 | V |
| | | M (falling) | 4.250 | 4.375 | 4.500 | |
| | | T (falling) | 3.000 | 3.075 | 3.150 | |
| | | S (falling) | 2.850 | 2.925 | 3.000 | |
| | | R (falling) | 2.550 | 2.625 | 2.700 | |
| | | Z (falling) | 2.250 | 2.313 | 2.375 | |
| | | Y (falling) | 2.125 | 2.188 | 2.250 | |
| | | W (falling) | 1.620 | 1.665 | 1.710 | |
| | | V (falling) | 1.530 | 1.575 | 1.620 | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}1$ = $V_{CC}2$ = +0.8V to +5.5V, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{CC}2$ Reset Threshold | $V_{TH}2$ | T (falling) | 3.000 | 3.075 | 3.150 | V |
| | | S (falling) | 2.850 | 2.925 | 3.000 | |
| | | R (falling) | 2.550 | 2.625 | 2.700 | |
| | | Z (falling) | 2.250 | 2.313 | 2.375 | |
| | | Y (falling) | 2.125 | 2.188 | 2.250 | |
| | | W (falling) | 1.620 | 1.665 | 1.710 | |
| | | V (falling) | 1.530 | 1.575 | 1.620 | |
| | | I (falling) | 1.350 | 1.388 | 1.425 | |
| | | H (falling) | 1.275 | 1.313 | 1.350 | |
| | | G (falling) | 1.080 | 1.110 | 1.140 | |
| | | F (falling) | 1.020 | 1.050 | 1.080 | |
| | | E (falling) | 0.810 | 0.833 | 0.855 | |
| | | D (falling) | 0.765 | 0.788 | 0.810 | |
| Reset Threshold Tempco | | | | 20 | | ppm/°C |
| Reset Threshold Hysteresis | $V_{HYST}$ | Referenced to $V_{TH}$ typical | | 0.5 | | % |
| $V_{CC_}$ to $\overline{RST}$ Output Delay | $t_{RD}$ | $V_{CC}1$ = ($V_{TH}1$ + 100mV) to ($V_{TH}1$ - 100mV) or $V_{CC}2$ = ($V_{TH}2$ + 75mV) to ($V_{TH}2$ - 75mV) | | 45 | | µs |
| Reset Timeout Period | $t_{RP}$ | D1 | 1.1 | 1.65 | 2.2 | ms |
| | | D2 | 8.8 | 13.2 | 17.6 | |
| | | D3 | 140 | 210 | 280 | |
| | | D5 | 280 | 420 | 560 | |
| | | D6 | 560 | 840 | 1120 | |
| | | D4 | 1120 | 1680 | 2240 | |
| **ADJUSTABLE RESET COMPARATOR INPUT (MAX6734A/MAX6735A)** | | | | | | |
| RSTIN Input Threshold | $V_{RSTIN}$ | | 611 | 626.5 | 642 | mV |
| RSTIN Input Current | $I_{RSTIN}$ | | -100 | | +100 | nA |
| RSTIN Hysteresis | | | | 3 | | mV |
| RSTIN to Reset Output Delay | $t_{RSTIND}$ | $V_{RSTIN}$ to ($V_{RSTIN}$ - 30mV) | | 22 | | µs |
| **MANUAL RESET INPUT (MAX6730A/MAX6731A/MAX6734A/MAX6735A)** | | | | | | |
| $\overline{MR}$ Input Threshold | $V_{IL}$ | | | | 0.3 × $V_{CC}1$ | V |
| | $V_{IH}$ | | 0.7 × $V_{CC}1$ | | | |
| $\overline{MR}$ Minimum Pulse Width | | | 1 | | | µs |
| $\overline{MR}$ Glitch Rejection | | | | 100 | | ns |
| $\overline{MR}$ to Reset Output Delay | $t_{MR}$ | | | 200 | | ns |
| $\overline{MR}$ Pullup Resistance | | | 25 | 50 | 80 | kΩ |

# Single-/Dual-/Triple-Voltage µP Supervisory Circuits with Independent Watchdog Output

## ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}1$ = $V_{CC}2$ = +0.8V to +5.5V, $T_A$ = -40°C to +125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

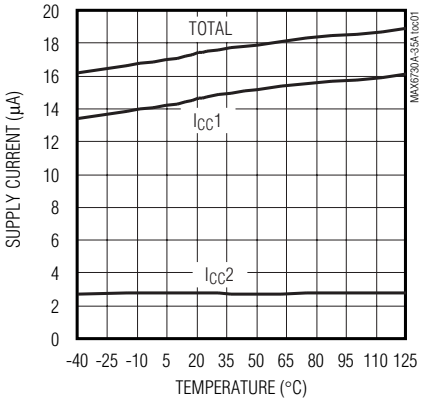
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **WATCHDOG INPUT** | | | | | | |
| Watchdog Timeout Period | $t_{WD-L}$ | First watchdog period after reset timeout period | 35 | 54 | 72 | s |
| | $t_{WD-S}$ | Normal mode | 1.12 | 1.68 | 2.24 | |
| WDI Pulse Width | $t_{WDI}$ | (Note 2) | 50 | | | ns |
| WDI Input Voltage | $V_{IL}$ | | | | $0.3 \times V_{CC}1$ | V |
| | $V_{IH}$ | | $0.7 \times V_{CC}1$ | | | |
| WDI Input Current | $I_{WDI}$ | WDI = 0V or $V_{CC}1$ | -1 | | +1 | µA |
| **RESET/WATCHDOG OUTPUT** | | | | | | |
| $\overline{RST}$/$\overline{WDO}$ Output Low Voltage (Push-Pull or Open Drain) | $V_{OL}$ | $V_{CC}1$ or $V_{CC}2$ ≥ +0.8V, $I_{SINK}$ = 1µA, output asserted | | | 0.3 | V |
| | | $V_{CC}1$ or $V_{CC}2$ ≥ +1.0V, $I_{SINK}$ = 50µA, output asserted | | | 0.3 | |
| | | $V_{CC}1$ or $V_{CC}2$ ≥ +1.2V, $I_{SINK}$ = 100µA, output asserted | | | 0.3 | |
| | | $V_{CC}1$ or $V_{CC}2$ ≥ +2.7V, $I_{SINK}$ = 1.2mA, output asserted | | | 0.3 | |
| | | $V_{CC}1$ or $V_{CC}2$ ≥ +4.5V, $I_{SINK}$ = 3.2mA, output asserted | | | 0.4 | |
| $\overline{RST}$/$\overline{WDO}$ Output High Voltage (Push-Pull Only) | $V_{OH}$ | $V_{CC}1$ ≥ +1.8V, $I_{SOURCE}$ = 200µA, output not asserted | $0.8 \times V_{CC}1$ | | | V |
| | | $V_{CC}1$ ≥ +2.7V, $I_{SOURCE}$ = 500µA, output not asserted | $0.8 \times V_{CC}1$ | | | |
| | | $V_{CC}1$ ≥ +4.5V, $I_{SOURCE}$ = 800µA, output not asserted | $0.8 \times V_{CC}1$ | | | |
| $\overline{RST}$/$\overline{WDO}$ Output Open-Drain Leakage Current | | Output not asserted | | | 0.5 | µA |

**Note 1:** Devices tested at $T_A$ = +25°C. Overtemperature limits are guaranteed by design and not production tested.
**Note 2:** Parameter guaranteed by design.

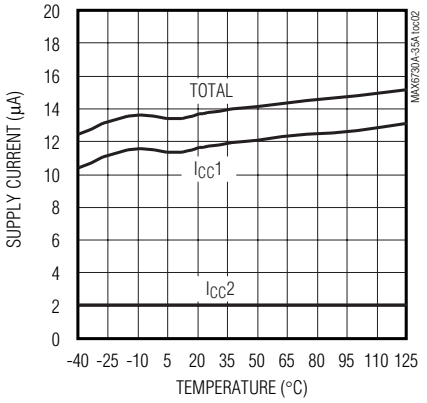
## Typical Operating Characteristics

($V_{CC}1$ = +5V, $V_{CC}2$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

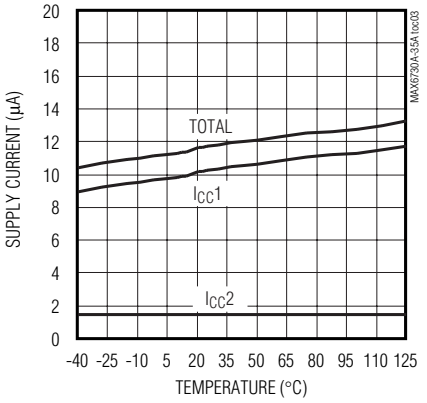
**SUPPLY CURRENT vs. TEMPERATURE ($V_{CC}1$ = +5V, $V_{CC}2$ = +3.3V)**



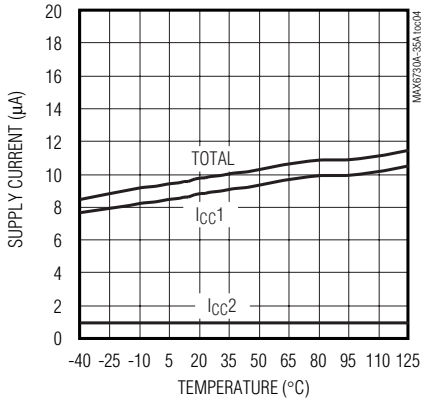

**SUPPLY CURRENT vs. TEMPERATURE ($V_{CC}1$ = +3.3V, $V_{CC}2$ = +2.5V)**



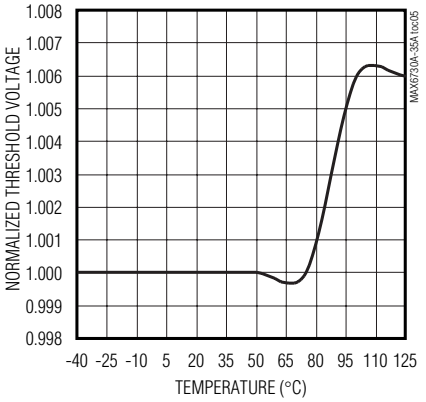

**SUPPLY CURRENT vs. TEMPERATURE ($V_{CC}1$ = +2.5V, $V_{CC}2$ = +1.8V)**




**SUPPLY CURRENT vs. TEMPERATURE ($V_{CC}1$ = +1.8V, $V_{CC}2$ = +1.2V)**




**NORMALIZED THRESHOLD VOLTAGE vs. TEMPERATURE**

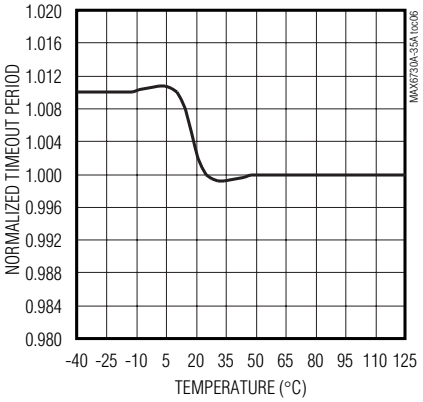


# Single-/Dual-/Triple-Voltage µP Supervisory Circuits with Independent Watchdog Output

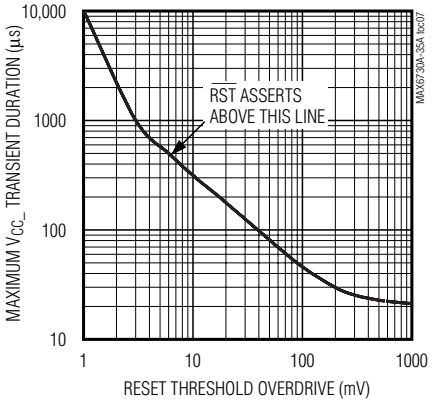
## Typical Operating Characteristics (continued)

($V_{CC}1$ = +5V, $V_{CC}2$ = +3.3V, $T_A$ = +25°C, unless otherwise noted.)

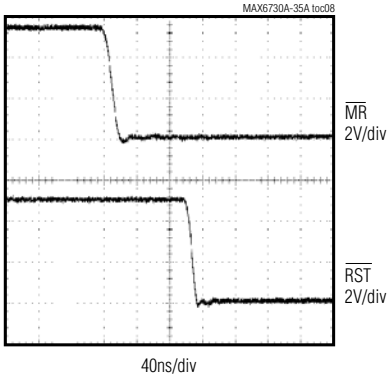
**NORMALIZED TIMEOUT PERIOD vs. TEMPERATURE**



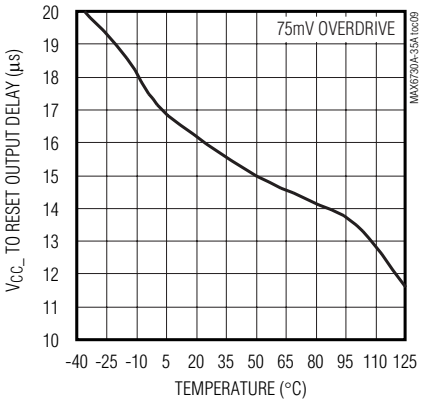

**MAXIMUM $V_{CC}$_ TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE**



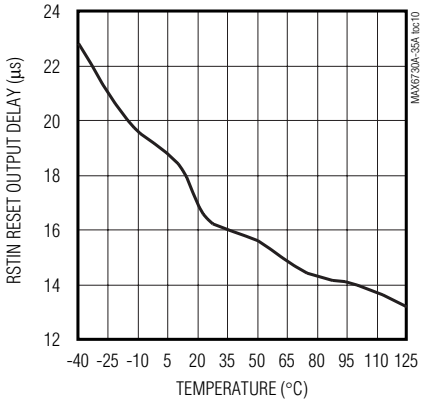

**$\overline{MR}$ TO RESET OUTPUT DELAY**




**$V_{CC}$_ TO RESET OUTPUT DELAY vs. TEMPERATURE**




**RSTIN TO RESET OUTPUT DELAY vs. TEMPERATURE**



## Pin Description

| PIN | | | NAME | FUNCTION |
|---|---|---|---|---|
| MAX6730A MAX6731A | MAX6732A MAX6733A | MAX6734A MAX6735A | | |
| 1 | 1 | 1 | $\overline{RST}$ | Active-Low Reset Output. The MAX6730A/MAX6732A/MAX6734A provide an open-drain output. The MAX6731A/MAX6733A/MAX6735A provide a push-pull output. $\overline{RST}$ asserts low when any of the following conditions occur: $V_{CC}1$ or $V_{CC}2$ drops below its preset threshold, RSTIN drops below its reset threshold, or $\overline{MR}$ is driven low. Open-drain versions require an external pullup resistor. |
| 2 | 2 | 2 | GND | Ground |
| 3 | 3 | 4 | $\overline{WDO}$ | Active-Low Watchdog Output. The MAX6730A/MAX6732A/MAX6734A provide an open-drain $\overline{WDO}$ output. The MAX6731A/MAX6733A/MAX6735A provide a push-pull $\overline{WDO}$ output. $\overline{WDO}$ asserts low when no low-to-high or high-to-low transition occurs on WDI within the watchdog timeout period ($t_{WD}$) or if an undervoltage-lockout condition exists for $V_{CC}1$, $V_{CC}2$, or RSTIN. $\overline{WDO}$ deasserts without a timeout period when $V_{CC}1$, $V_{CC}2$, and RSTIN exceed their reset thresholds, or when the manual reset input is deasserted. Open-drain versions require an external pullup resistor. |
| 4 | — | 5 | $\overline{MR}$ | Active-Low Manual Reset Input. Drive $\overline{MR}$ low to force a reset. $\overline{RST}$ remains asserted as long as $\overline{MR}$ is low and for the reset timeout period after $\overline{MR}$ releases high. $\overline{MR}$ has a 50kΩ pullup resistor to $V_{CC}1$; leave $\overline{MR}$ open or connect to $V_{CC}1$ if unused. |
| 5 | 5 | 3 | WDI | Watchdog Input. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer expires and the watchdog output asserts low. The internal watchdog timer clears whenever $\overline{RST}$ asserts or a rising or falling edge on WDI is detected. The watchdog has an initial watchdog timeout period (35s min) after each reset event and a short timeout period (1.12s min) after the first valid WDI transition. Floating WDI does not disable the watchdog timer function. |
| 6 | 6 | 8 | $V_{CC}1$ | Primary Supply-Voltage Input. $V_{CC}1$ provides power to the device when it is greater than $V_{CC}2$. $V_{CC}1$ is the input to the primary reset threshold monitor. |
| — | 4 | 6 | $V_{CC}2$ | Secondary Supply-Voltage Input. $V_{CC}2$ provides power to the device when it is greater than $V_{CC}1$. $V_{CC}2$ is the input to the secondary reset threshold monitor. |
| — | — | 7 | RSTIN | Undervoltage Reset Comparator Input. RSTIN provides a high-impedance comparator input for the adjustable reset monitor. $\overline{RST}$ asserts low if the voltage at RSTIN drops below the 626mV internal reference voltage. Connect a resistive voltage-divider to RSTIN to monitor voltages higher than 626mV. Connect RSTIN to $V_{CC}1$ or $V_{CC}2$ if unused. |

# Single-/Dual-/Triple-Voltage µP Supervisory Circuits with Independent Watchdog Output

**Table 1. Reset Voltage Threshold Suffix Guide****

| PART NUMBER SUFFIX | $V_{CC}1$ NOMINAL VOLTAGE THRESHOLD(V) | $V_{CC}2$ NOMINAL VOLTAGE THRESHOLD (V) |
|---|---|---|
| **LT** | **4.625** | **3.075** |
| MS | 4.375 | 2.925 |
| MR | 4.375 | 2.625 |
| TZ | 3.075 | 2.313 |
| **SY** | **2.925** | **2.188** |
| RY | 2.625 | 2.188 |
| TW | 3.075 | 1.665 |
| **SV** | **2.925** | **1.575** |
| **RV** | **2.625** | **1.575** |
| TI | 3.075 | 1.388 |
| **SH** | **2.925** | **1.313** |
| RH | 2.625 | 1.313 |
| **TG** | **3.075** | **1.110** |
| SF | 2.925 | 1.050 |
| RF | 2.625 | 1.050 |
| TE | 3.075 | 0.833 |
| **SD** | **2.925** | **0.788** |
| RD | 2.625 | 0.788 |
| **ZW** | **2.313** | **1.665** |
| YV | 2.188 | 1.575 |
| ZI | 2.313 | 1.388 |
| **YH** | **2.188** | **1.313** |
| **ZG** | **2.313** | **1.110** |
| YF | 2.188 | 1.050 |
| ZE | 2.313 | 0.833 |
| **YD** | **2.188** | **0.788** |
| WI | 1.665 | 1.388 |
| **VH** | **1.575** | **1.313** |
| **WG** | **1.665** | **1.110** |
| VF | 1.575 | 1.050 |
| WE | 1.665 | 0.833 |
| **VD** | **1.575** | **0.788** |

***Standard versions are shown in bold and are available in a D3 timeout option only. Standard versions require 2500-piece order increments and are typically held in sample stock. There is a 10,000-piece order increment on nonstandard versions.*
***Other threshold voltages may be available; contact factory for availability.***

**Table 2. Reset Timeout Period Suffix Guide**

| TIMEOUT PERIOD SUFFIX | ACTIVE TIMEOUT PERIOD | |
|---|---|---|
| | MIN (ms) | MAX (ms) |
| D1 | 1.1 | 2.2 |
| D2 | 8.8 | 17.6 |
| D3 | 140 | 280 |
| D5 | 280 | 560 |
| D6 | 560 | 1120 |
| D4 | 1120 | 2240 |

## Detailed Description

### Supply Voltages

The MAX6730A–MAX6735A microprocessor (µP) supervisors maintain system integrity by alerting the µP to fault conditions. The MAX6730A–MAX6735A monitor one to three supply voltages in µP-based systems and assert an active-low reset output when any monitored supply voltage drops below its preset threshold. The output state remains valid for $V_{CC}1$ or $V_{CC}2$ greater than +0.8V.

### Threshold Levels

The two-letter code in the Reset Voltage Threshold Suffix Guide (Table 1) indicates the threshold level combinations for $V_{CC}1$ and $V_{CC}2$.

### Reset Output

The MAX6730A–MAX6735A feature an active-low reset output ($\overline{RST}$). $\overline{RST}$ asserts when the voltage at either $V_{CC}1$ or $V_{CC}2$ falls below the voltage threshold level, $V_{RSTIN}$ drops below its threshold, or $\overline{MR}$ is driven low (Figure 1). $\overline{RST}$ remains low for the reset timeout period (Table 2) after $V_{CC}1$, $V_{CC}2$, and RSTIN increase above their respective thresholds and after $\overline{MR}$ releases high. Whenever $V_{CC}1$, $V_{CC}2$, or RSTIN go below the reset threshold before the end of the reset timeout period, the internal timer restarts. The MAX6730A/MAX6732A/MAX6734A provide an open-drain $\overline{RST}$ output, and the MAX6731A/MAX6733A/MAX6735A provide a push-pull $\overline{RST}$ output.

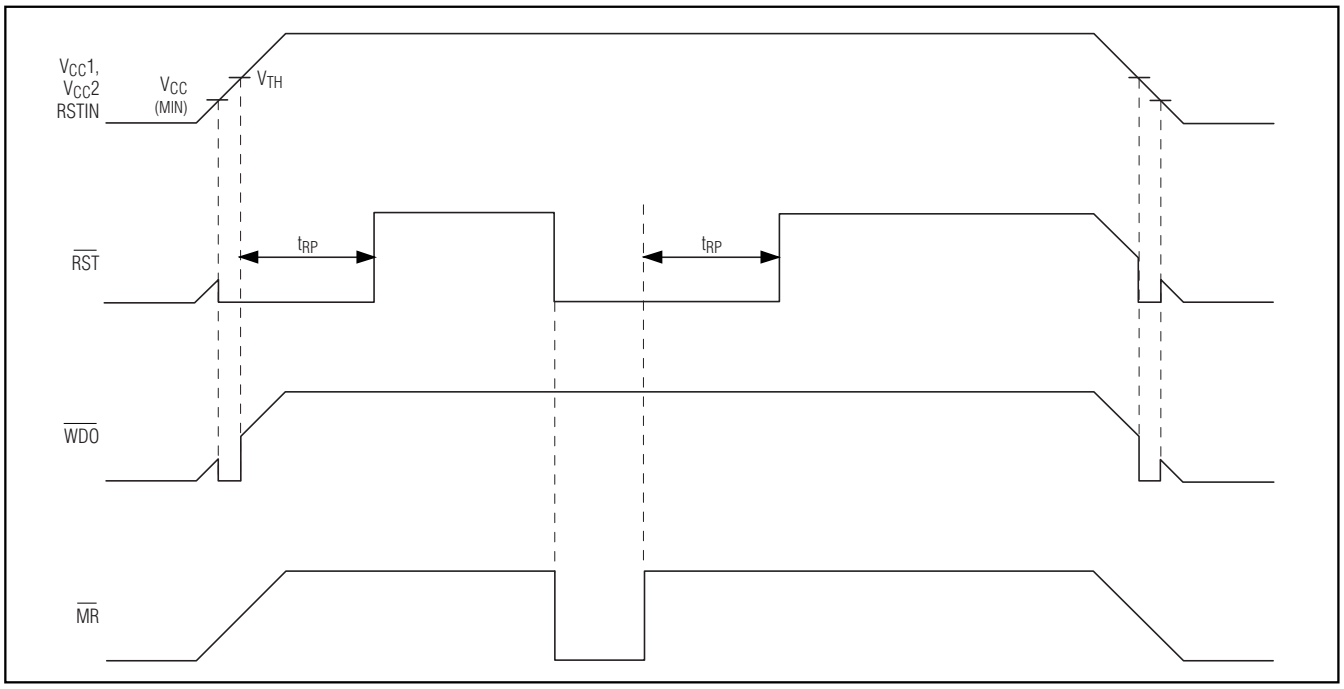



*Figure 1. $\overline{RST}$, $\overline{WDO}$, and $\overline{MR}$ Timing Diagram*

### Manual Reset Input

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic-low on $\overline{MR}$ asserts the reset output, clears the watchdog timer, and deasserts the watchdog output. Reset remains asserted while $\overline{MR}$ is low and for the reset timeout period ($t_{RP}$) after $\overline{MR}$ returns high. An internal 50kΩ pullup resistor allows $\overline{MR}$ to be left open if unused. Drive $\overline{MR}$ with CMOS-logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. Connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity when driving $\overline{MR}$ over long cables or if the device is used in a noisy environment.

### Adjustable Input Voltage (RSTIN)

The MAX6734A/MAX6735A provide an additional high-impedance comparator input with a 626mV threshold to monitor a third supply voltage. To monitor a voltage higher than 626mV, connect a resistive divider to the circuit as shown in Figure 2 to establish an externally controlled threshold voltage, $V_{EXT_TH}$.

$$V_{EXT_TH} = 626mV \times \frac{(R1+R2)}{R2}$$

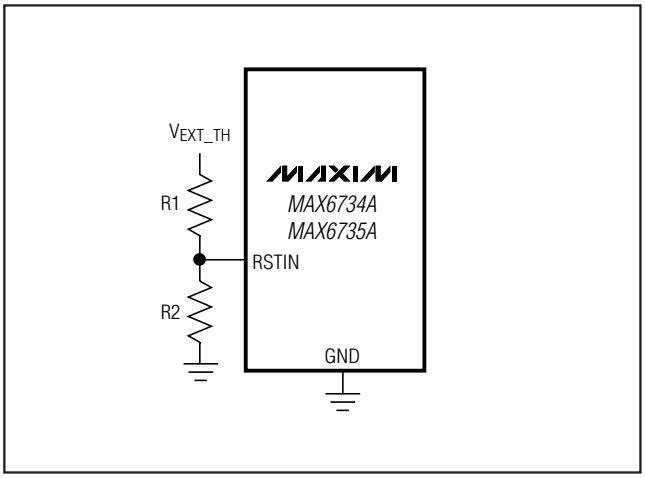



*Figure 2. Monitoring a Third Voltage*

# Single-/Dual-/Triple-Voltage µP Supervisory Circuits with Independent Watchdog Output

The RSTIN comparator derives power from $V_{CC}1$, and the input voltage must remain less than or equal to $V_{CC}1$. Low leakage current at RSTIN allows the use of large-valued resistors, resulting in reduced power consumption of the system.

### Watchdog

The watchdog feature monitors µP activity through the watchdog input (WDI). A rising or falling edge on WDI within the watchdog timeout period ($t_{WD}$) indicates normal µP operation. $\overline{WDO}$ asserts low if WDI remains high or low for longer than the watchdog timeout period. Floating WDI does not disable the watchdog timer.

The MAX6730A–MAX6735A include a dual-mode watchdog timer to monitor µP activity. The flexible timeout architecture provides a long-period initial watchdog mode, allowing complicated systems to complete lengthy boots, and a short-period normal watchdog mode, allowing the supervisor to provide quick alerts when processor activity fails. After each reset event ($V_{CC}$ power-up, brownout, or manual reset), there is a long initial watchdog period of 35s (min). The long watchdog period mode provides an extended time for the system to power up and fully initialize all µP and system components before assuming responsibility for routine watchdog updates.

The usual watchdog timeout period (1.12s min) begins after the initial watchdog timeout period ($t_{WD-L}$) expires or after the first transition on WDI (Figure 3). During normal operating mode, the supervisor asserts the $\overline{WDO}$ output if the µP does not update the WDI with a valid transition (high to low or low to high) within the standard timeout period ($t_{WD-S}$) (1.12s min).

Connect $\overline{MR}$ to $\overline{WDO}$ to force a system reset in the event that no rising or falling edge is detected at WDI within the watchdog timeout period. $\overline{WDO}$ asserts low when no edge is detected by WDI, the $\overline{RST}$ output asserts low, the watchdog counter immediately clears, and $\overline{WDO}$ returns high. The watchdog counter restarts, using the long watchdog period, when the reset timeout period ends (Figure 4).

### Ensuring a Valid Reset Output Down to $V_{CC}$ = 0V

The MAX6730A–MAX6735A guarantee proper operation down to $V_{CC}$ = +0.8V. In applications that require valid reset levels down to $V_{CC}$ = 0V, use a 100kΩ pull-down resistor from $\overline{RST}$ to GND. The resistor value used is not critical, but it must be large enough not to load the reset output when $V_{CC}$ is above the reset threshold. For most applications, 100kΩ is adequate. Note that this configuration does not work for the open-drain outputs of MAX6730A/MAX6732A/MAX6734A.

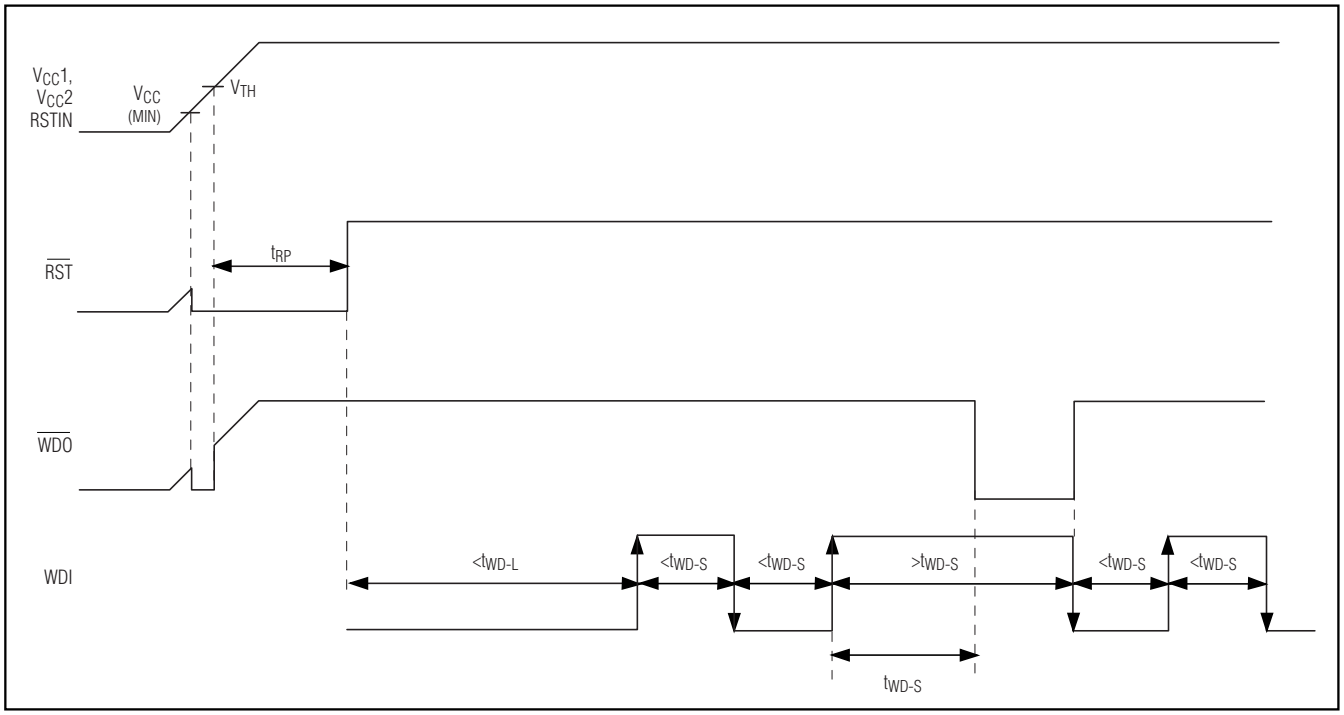



*Figure 3. Watchdog Input/Output Timing Diagram ($\overline{MR}$ and $\overline{WDO}$ Not Connected)*

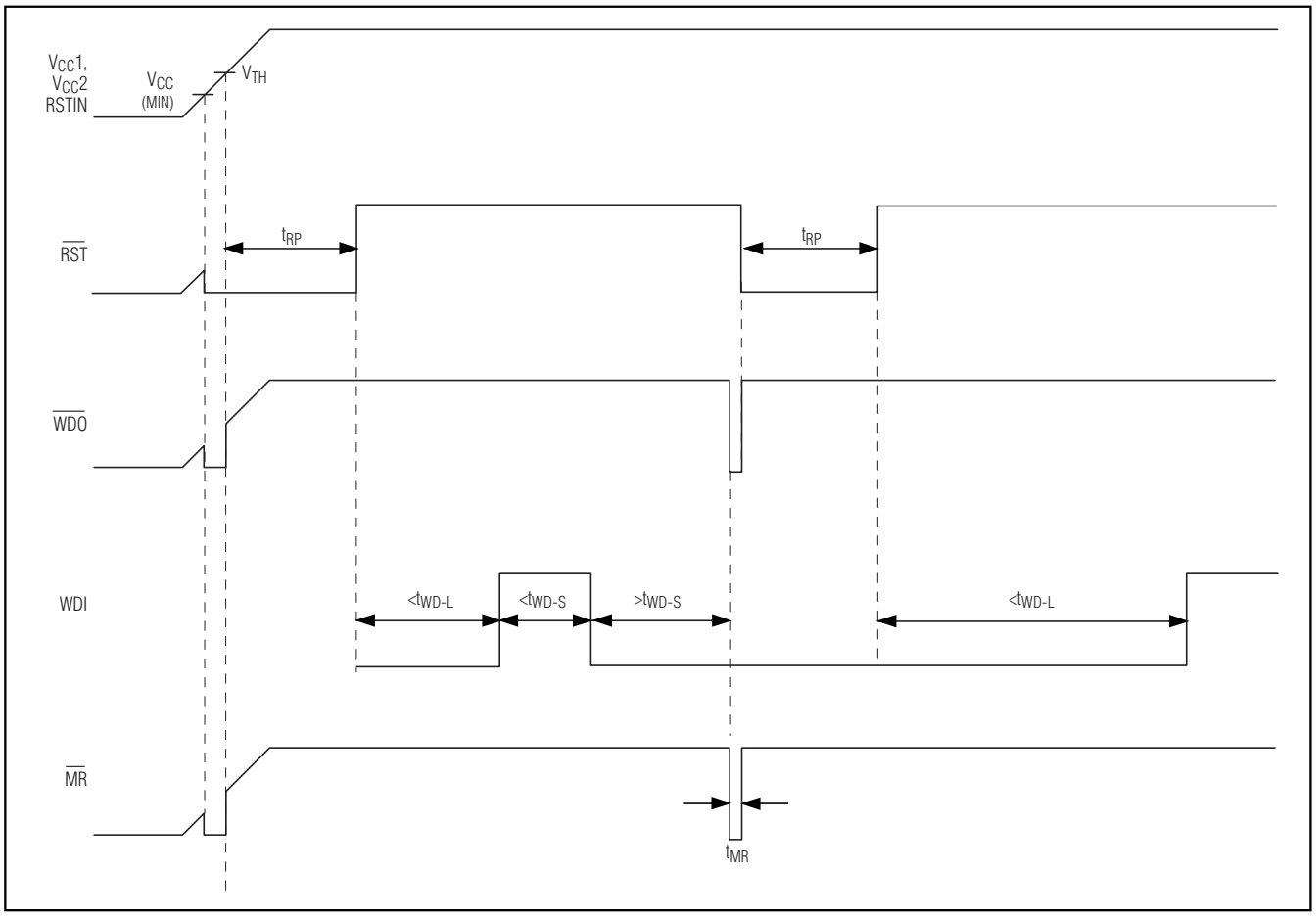



*Figure 4. Watchdog Input/Output Timing Diagram (MR and WDO Connected)*

## Applications Information

### Interfacing to µPs with Bidirectional Reset Pins

Microprocessors with bidirectional reset pins can interface directly with the open-drain RST output options. However, conditions might occur in which the push-pull output versions experience logic contention with the bidirectional reset pin of the µP. Connect a 10kΩ resistor between RST and the µP's reset I/O port to prevent logic contention (Figure 5).

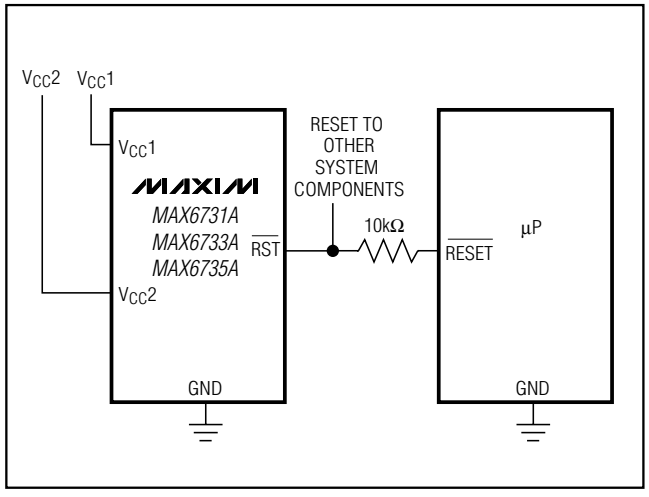



*Figure 5. Interfacing to µPs with Bidirectional Reset I/O*

### Falling VCC Transients

The MAX6730A–MAX6735A µP supervisors are relatively immune to short-duration falling VCC_ transients (glitches). Small glitches on VCC_ are ignored by the MAX6730A–MAX6735A, preventing undesirable reset pulses to the µP. The *Typical Operating Characteristics* show Maximum VCC_ Transient Duration vs. Reset

# Single-/Dual-/Triple-Voltage µP Supervisory Circuits with Independent Watchdog Output

Threshold Overdrive graph, for which reset pulses are not generated. The graph was produced using falling $V_{CC_}$ pulses, starting above $V_{TH}$ and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a falling $V_{CC}$ transient typically might have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes further below the reset threshold), the maximum allowable pulse width decreases. A 0.1µF bypass capacitor mounted close to $V_{CC_}$ provides additional transient immunity.

### Watchdog Software Considerations

Setting and resetting the watchdog input at different points in the program rather than "pulsing" the watchdog input high-low-high or low-high-low helps the watchdog timer closely monitor software execution. This technique avoids a "stuck" loop, in which the watchdog timer continues to be reset within the loop, preventing the watchdog from timing out. Figure 6 shows an example flow diagram in which the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, and then set high again when the program returns to the beginning. If the program "hangs" in any subroutine, the I/O continually asserts low (or high), and the watchdog timer expires, issuing a reset or interrupt.

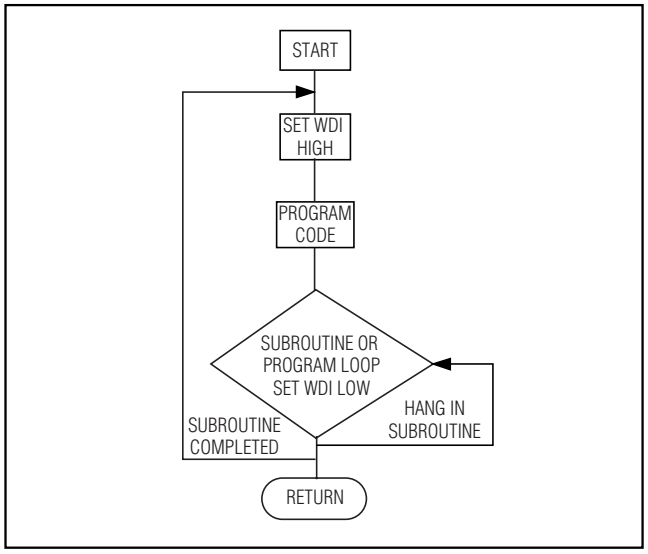
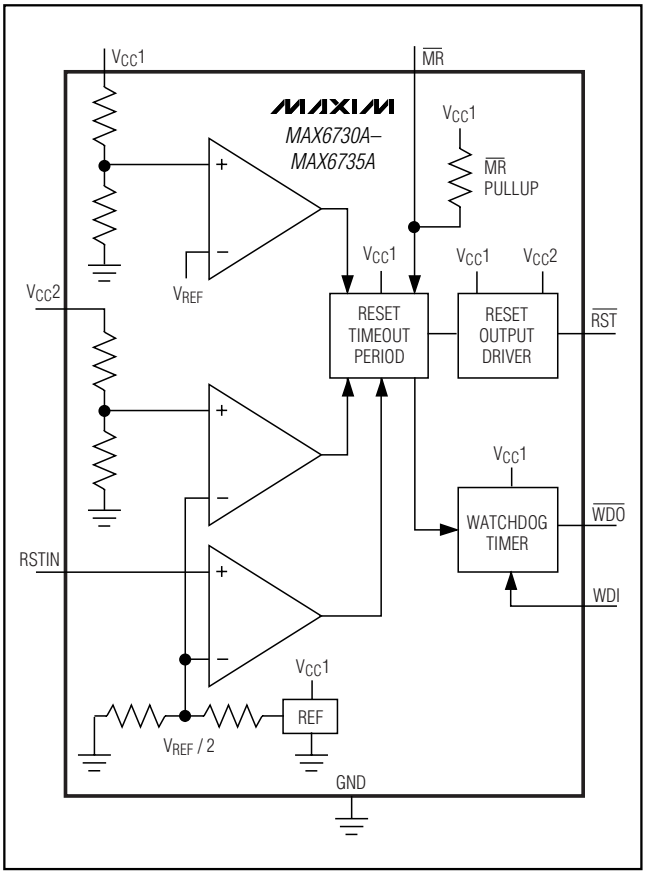



*Figure 6. Watchdog Flow Diagram*

## Functional Diagram



## Standard Versions

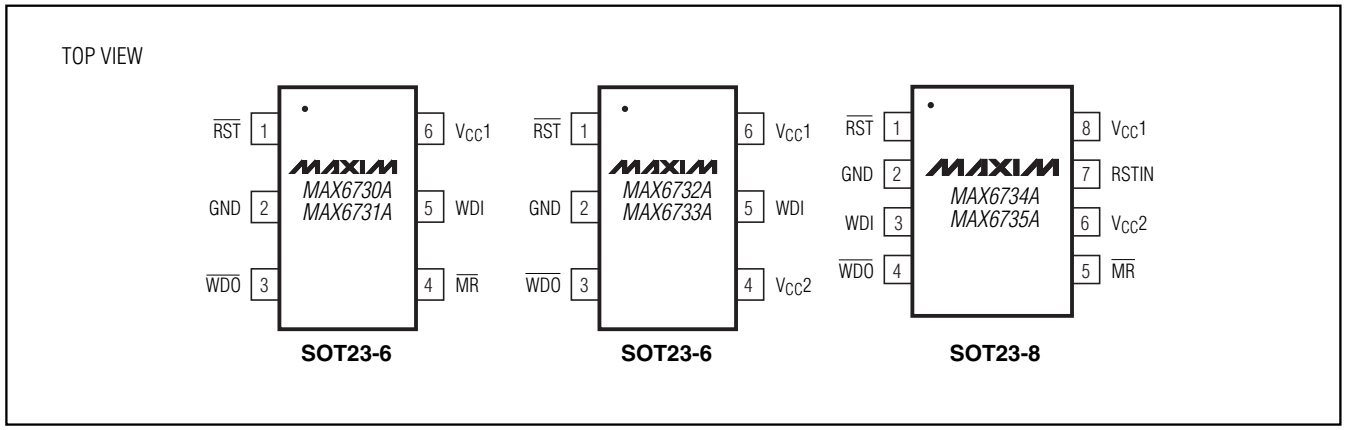
| PART | TOP MARK |
|---|---|
| **MAX6730A**UTLD3-T | +ACIX |
| MAX6730AUTSD3-T | +ACJA |
| MAX6730AUTRD3-T | +ACIY |
| MAX6730AUTZD3-T | +ACJF |
| MAX6730AUTVD3-T | +ACJC |
| **MAX6731A**UTLD3-T | +ACJG |
| MAX6731AUTTD3-T | +ACJJ |
| MAX6731AUTSD3-T | +ACJI |
| MAX6731AUTRD3-T | +ACJH |
| MAX6731AUTZD3-T | +ACJL |
| MAX6731AUTVD3-T | +ACJK |
| **MAX6732A**UTLTD3-T | +ACHU |
| MAX6732AUTSYD3-T | +ACHZ |
| MAX6732AUTSVD3-T | +ACHY |
| MAX6732AUTRVD3-T | +ACHV |
| MAX6732AUTSHD3-T | +ACHX |
| MAX6732AUTTGD3-T | +ACIA |
| MAX6732AUTSDD3-T | +ACHW |
| MAX6732AUTZWD3-T | +ACIH |
| MAX6732AUTYHD3-T | +ACIF |
| MAX6732AUTZGD3-T | +ACIG |
| MAX6732AUTYDD3-T | +ACIE |
| MAX6732AUTVHD3-T | +ACIC |
| MAX6732AUTWGD3-T | +ACID |
| MAX6732AUTVDD3-T | +ACIB |
| **MAX6733A**UTLTD3-T | +ACII |
| MAX6733AUTSYD3-T | +ACIN |
| MAX6733AUTSVD3-T | +ACIM |
| MAX6733AUTRVD3-T | +ACIJ |
| MAX6733AUTSHD3-T | +ACIL |
| MAX6733AUTTGD3-T | +ACIO |
| MAX6733AUTSDD3-T | +ACIK |
| MAX6733AUTZWD3-T | +ACIW |
| MAX6733AUTYHD3-T | +ACIU |

| PART | TOP MARK |
|---|---|
| MAX6733AUTZGD3-T | +ACIV |
| MAX6733AUTYDD3-T | +ACIT |
| MAX6733AUTVHD3-T | +ACIR |
| MAX6733AUTWGD3-T | +ACIS |
| MAX6733AUTVDD3-T | +ACIQ |
| **MAX6734A**KALTD3-T | +AENS |
| MAX6734AKASYD3-T | +AENZ |
| MAX6734AKASVD3-T | +AENY |
| MAX6734AKARVD3-T | +AENU |
| MAX6734AKASHD3-T | +AENX |
| MAX6734AKATGD3-T | +AEOA |
| MAX6734AKASDD3-T | +AENV |
| MAX6734AKAZWD3-T | +AEOI |
| MAX6734AKAYHD3-T | +AEOG |
| MAX6734AKAZGD3-T | +AEOH |
| MAX6734AKAYDD3-T | +AEOF |
| MAX6734AKAVHD3-T | +AEOD |
| MAX6734AKAWGD3-T | +AEOE |
| MAX6734AKAVDD3-T | +AEOC |
| **MAX6735A**KALTD3-T | +AEOJ |
| MAX6735AKASYD3-T | +AEOO |
| MAX6735AKASVD3-T | +AEON |
| MAX6735AKARVD3-T | +AEOK |
| MAX6735AKASHD3-T | +AEOM |
| MAX6735AKATGD3-T | +AEOP |
| MAX6735AKASDD3-T | +AEOL |
| MAX6735AKAZWD3-T | +AEOX |
| MAX6735AKAZID3-T | +AEOW |
| MAX6735AKAYHD3-T | +AEOU |
| MAX6735AKAZGD3-T | +AEOV |
| MAX6735AKAYDD3-T | +AEOT |
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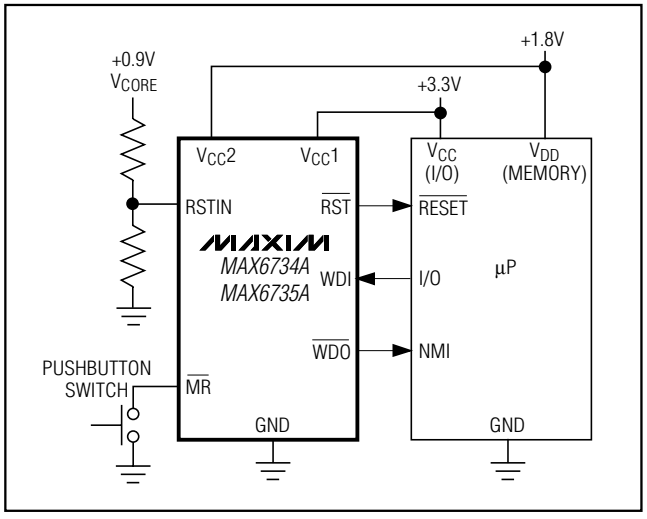
***Note:*** *Sample stock is generally held on standard versions only. Standard versions have an order increment requirement of 2500 pieces. Nonstandard versions have an order increment requirement of 10,000 pieces. Contact factory for availability of nonstandard versions.*

# Single-/Dual-/Triple-Voltage µP Supervisory Circuits with Independent Watchdog Output

## Pin Configurations




## Typical Operating Circuit




## Chip Information

TRANSISTOR COUNT: 1073

PROCESS: BiCMOS

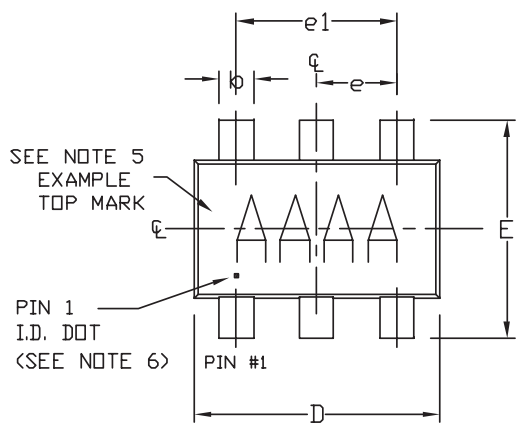
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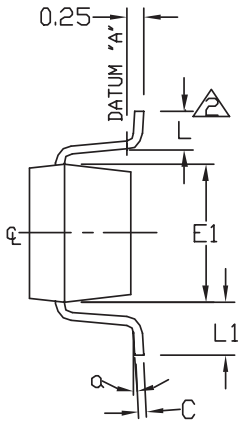
| PART NUMBER | VOLTAGE MONITORS | $\overline{\text{RST}}$ OUTPUT | MANUAL RESET | WATCHDOG INPUT | WATCHDOG OUTPUT |
|---|---|---|---|---|---|
| MAX6730A | 1 | Open Drain | √ | √ | Open Drain |
| MAX6731A | 1 | Push-Pull | √ | √ | Push-Pull |
| MAX6732A | 2 | Open Drain | — | √ | Open Drain |
| MAX6733A | 2 | Push-Pull | — | √ | Push-Pull |
| MAX6734A | 3 | Open Drain | √ | √ | Open Drain |
| MAX6735A | 3 | Push-Pull | √ | √ | Push-Pull |

## Package Information

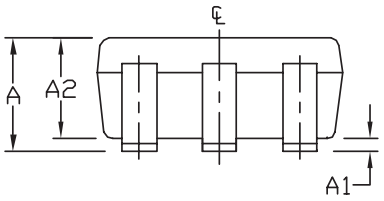
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

6LSOT.EPS




| SYMBOL | MIN | MAX |
|---|---|---|
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.35 | 0.50 |
| C | 0.08 | 0.20 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.75 |
| L | 0.35 | 0.60 |
| L1 | 0.60 REF. | |
| e1 | 1.90 BSC. | |
| e | 0.95 BSC. | |
| α | 0° | 10° |




NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1 MM.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

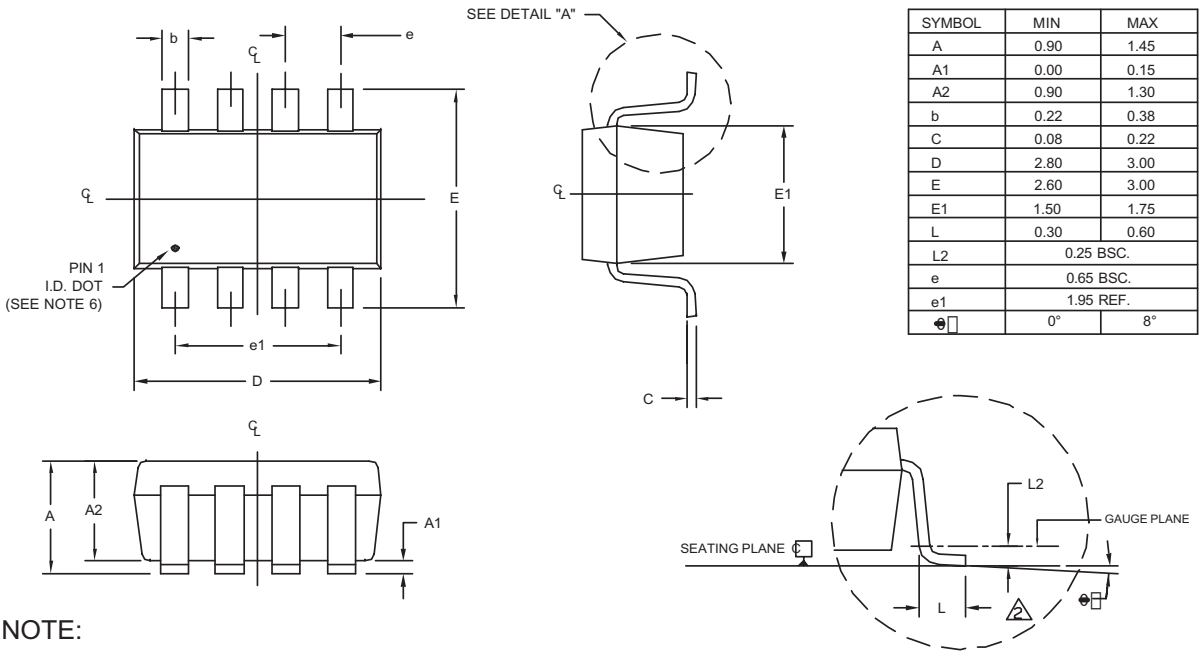
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|---|---|---|---|
| APPROVAL | DOCUMENT CONTROL NO. 21-0058 | REV. G | 1/1 |

# Single-/Dual-/Triple-Voltage µP Supervisory Circuits with Independent Watchdog Output

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOT23, 8L .EPS




| SYMBOL | MIN | MAX |
|---|---|---|
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.22 | 0.38 |
| C | 0.08 | 0.22 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.75 |
| L | 0.30 | 0.60 |
| L2 | 0.25 BSC. | |
| e | 0.65 BSC. | |
| e1 | 1.95 REF. | |
| θ | 0° | 8° |

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT IS 0.3 MM Ø MIN. LOCATED ABOVE PIN 1.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178 VARIATION BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0078 | E | 1/1 |

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